UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,997	08/07/2001	Hiroyuki Takahashi	SIM-01501	1911

26339 7590 03/10/2004

PATENT GROUP
CHOATE, HALL & STEWART
EXCHANGE PLACE, 53 STATE STREET
BOSTON, MA 02109

EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,997	TAKAHASHI, HIROYUKI	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15,19-24 and 27-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 22-24* is/are allowed.

6)☒ Claim(s) *19-21 and 27-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *09 May 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

`DETAILED ACTION

1. Applicant's arguments filed 12/04/03 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 19 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 19, lines 12-15 add the limitation "wherein, when the logic signal is fixed at a low level during a standby state, one of said first capacitor and said second capacitor is set to an off-state in response to a chip select signal controlling said standby state, and the other of said first capacitor and said second capacitor is set to an off-state in response to said chip select signal that is negated", which is seen to be new matter because the specification as originally filed does not support this limitation.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 29-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 29-31 are indefinite because the claims are misdescriptive. Claims 29-31 each claim that the corresponding gate (NOR, AND, NAND) is coupled to the first node and the 2n-th node. This is not what is shown in the figures, nor is it what applicant discloses in the statements given on page 14 of the response to show support for the claims. The figures show that the gates are connected to the first node and the (2n+1)-th node. In addition claim 29 is further misdescriptive because (with reference to Figure 4) the n-MOS capacitor is not coupled to an odd node, it is in fact coupled to an even node (node 2). This is the

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 19-21, 27, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (U.S. Patent No. 5,055,713).

In reference to claim 19, Watanabe discloses in Figure 5 a delay circuit comprising: first and second nodes; a first inverter (I2), the output of which is coupled to the first node, the first inverter (I2) receiving a logic signal; a second inverter (I3), the input of which is coupled to the first node and the output of which is coupled to the second node; a first capacitor (C1) coupled between the first node and a first power source line (VSS), the first capacitor (C1) being of a first channel type (n-MOS); and a second capacitor (C2) coupled between the second node and a second power source

line (VCC), the second capacitor (C2) being of a second channel type (p-MOS) which is different form the first channel type. The same applies to claim 21, wherein the first power source line (VSS) is fixed at a ground potential. The same also applies to claim 20 wherein the first transistor being a p-MOS and the second transistor being an n-MOS with the second power source line fixed at a ground potential is seen to be a design expedient dependent on the particular environment. It is considered well-known to those having skill in the art that the polarities could be reversed and the transistors switched from n-MOS to p-MOS and vice versa to achieve the same result.

In reference to claim 27, Watanabe discloses in Figure 5 a delay circuit for delaying a logic signal having a first logical level and a second logical level, comprising: an inverter chain (I4, I5) including a plurality of inverters and at least one first capacitor (C4), the inverter chain receiving the logic signal, the first capacitor including a MOS transistor of a first channel type (n-MOS), the first capacitor being operated so that the capacitor (C4) changes from an off-state to an on-state to increase it capacitance when the logic signal changes from a first logical level to a second logical level, whereby the inverter chain outputs a first delay signal generated after a first delay time from the transition timing from the first to the second logical levels of the logic signal, the first capacitor (C4) being operated so that the capacitor (C4) changes from an on-state to an off-state to decrease it capacitance when the logic signal changes from a second logical level to a first logical level, whereby the inverter chain outputs a second delay signal generated after a second delay time from the transition timing from the second to the first logical levels of the logic signal, the second delay time being shorter than the first

delay time, a logical gate (NA2) receiving the output of the inverter chain and the logic signal so that the logical gate outputs its output signal in response to the first delay signal when the logic signal changes from the first logical level to the second logical level.

In reference to claim 28, Watanabe further discloses in Figure 5 a second capacitor (C5), the second capacitor (C5) being comprised of a MOS transistor of a second channel type (p-MOS) which is different from the first channel type (n-MOS), the second capacitor being coupled to a node which is different from the node coupled to the first capacitor (C4) in the inverter chain, the second capacitor (C5) being operated so that the capacitor (C5) changes from an off-state to an on-state to increase it capacitance when the logic signal changes from a first logical level to a second logical level, whereby the inverter chain outputs a first delay signal generated after a first delay time from the transition timing from the first to the second logical levels of the logic signal, the second capacitor (C5) being operated so that the capacitor (C5) changes from an on-state to an off-state to decrease it capacitance when the logic signal changes from a second logical level to a first logical level, whereby the inverter chain outputs a second delay signal generated after a second delay time from the transition timing from the second to the first logical levels of the logic signal, the second delay time being shorter than the first delay time.

In reference to claim 29 Watanabe discloses in Figure 7, a delay circuit comprising: 2n+1 nodes (8) defined in series, n being a natural number, a first node (input of inverter I7) receiving a logical signal; 2n inverters (7), each inverter arranged

between adjacent nodes of said 2n+1 nodes; a capacitor (C12) of an n-MOS type coupled between an odd node (3) and a power source line; and a NOR gate (NG) coupled to the first node and the (2n+1)-th node, this is based on the examiner's understanding of the claim.

In reference to claim 31 Watanabe discloses in Figure 5, a delay circuit comprising: 2n+1 nodes (3) defined in series, n being a natural number, a first node receiving a logical signal, 2n inverters (2), each inverter arranged between adjacent nodes of said 2n+1 nodes; a capacitor (C1) of an n-MOS type coupled between an even node and a first power source line; a capacitor (C2) of a P-MOS type coupled between an odd node and a second power source line; and a NAND gate (NA1) coupled between the first node and the (2n+1)-th node, based on the examiner's understanding of the claim.

Response to Arguments

7. Applicant's arguments filed 12/04/03 have been fully considered but they are not persuasive. The applicant's arguments with respect to claim 19 are not persuasive because the claim appears to have added material that is not supported by the specification, therefore not patentable weight has been given to those limitations and the previous rejection has been repeated. In reference to applicant's argument with respect to claim 27 the rejection has been withdrawn and a new rejection has been stated.

Allowable Subject Matter

8. Claims 15 and 22-24 are allowed.

9. The following is an examiner's statement of reasons for allowance: Claim 15 is allowed because the closest prior art of record fails to disclose a circuit as disclosed in the specification page 31, line 15 through page 32, line 1 wherein the low threshold voltage n-MOS transistors of each of a first and a third inverter are connected to ground by a high threshold voltage n-MOS transistor; and low threshold voltage p-MOS transistors of each of a second and a fourth inverter are connected to ground by a high threshold p-MOS transistor; and said high threshold voltage n-MOS transistor and p-MOS transistor are set to an off state in response to a chip select signal and a chip select signal that is negated (respectively) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 22-24 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 2A wherein no capacitor is connected to the second node in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on alternate Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC
CC
March 7, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800